IN THE CLAIMS

Please Amend the Claims in accordance with the following markup:

1. (Currently Amended) A method for evaluating a shorting defect in an integrated circuit, said method comprising:

reading a plurality of quiescent power-plane current values at a plurality of corresponding power-plane voltages for a test vector for which said shorting defect is activated;

detecting a change in linearity of said plurality of power-plane current values with respect to said power-plane voltages;

determining a particular power-plane voltage above which said detecting detects that said plurality of power-plane current values are linear with respect to said power plane voltages; and

evaluating a level of severity of said shorting defect, wherein said level is determined in conformity with a value of said particular power-plane voltage ~~a result of said detecting~~.

2. (Canceled).

3. (Currently Amended) The method of Claim 1 ~~2~~, further comprising:

computing a first derivative of said quiescent power-plane current values at multiple ones of said power-plane voltages; and

detecting a peak value of said computed first derivative, and wherein said determining determines a ~~lower bound of said range~~ said particular power plane

voltage as a voltage corresponding to said peak value.

4. (Original) The method of Claim 1, further comprising:

second reading a second plurality of quiescent power-plane current values at said plurality of power-plane voltages for a second test vector for which said shorting defect is not activated; and

subtracting said second plurality of quiescent power-plane current values from said plurality of quiescent power-plane current values read by said reading, whereby said plurality of quiescent power-plane current values are normalized, and wherein said detecting is performed on said normalized quiescent power-plane current values.

5. (Original) The method of Claim 4, further comprising selecting a second test vector as a vector having a lowest power-plane quiescent current value at a predetermined operating voltage from among a set of test vectors.

6. (Original) The method of Claim 1, wherein said evaluating comprises:

determining whether or not a power-plane voltage corresponding to said change in linearity is above a predetermined threshold; and

in response to determining that voltage is above said predetermined threshold, rejecting said integrated circuit as a failure.

7. (Original) The method of Claim 1, further comprising selecting said test vector as a vector having a highest power-plane quiescent current value at a predetermined operating voltage from among a set of test vectors.

8. (Currently Amended) A computer program product for use with a workstation computer, wherein said computer program product comprises signal bearing media containing program instructions for execution within said workstation computer for evaluating a shorting defect in an integrated circuit, wherein said program instructions comprise program instructions for:

reading a plurality of quiescent power-plane current values at a plurality of corresponding power-plane voltages for a test vector for which said shorting defect is activated;

detecting a change in linearity of said plurality of power-plane current values with respect to said power-plane voltages;

determining a particular power-plane voltage above which said program instructions for detecting detect that said plurality of power-plane current values are linear with respect to said power-plane voltages; and

evaluating a level of severity of said shorting defect, wherein said level of severity is determined in conformity with said particular power-plane voltage ~~a result of said detecting~~.

9. (Canceled).

10. (Currently Amended) The computer program product of Claim 8 [[9]], wherein said program instructions further comprise program instructions for:

computing a first derivative of said quiescent power-plane current values at multiple ones of said power-plane voltages; and

detecting a peak value of said computed first

derivative, and wherein said program instructions for determining determine said particular power plane voltage ~~a lower bound of said range~~ as a voltage corresponding to said peak value.

11. (Original) The computer program product of Claim 8, wherein said program instructions further comprise program instructions for:

second reading a second plurality of quiescent power-plane current values at said plurality of power-plane voltages for a second test vector for which said shorting defect is not activated; and

subtracting said second plurality of quiescent power-plane current values from said plurality of quiescent power-plane current values read by said reading, whereby said plurality of quiescent power-plane current values are normalized, and wherein said program instructions for detecting operate on said normalized quiescent power-plane current values.

12. (Original) The computer program product of Claim 11, wherein said program instructions further comprise program instructions for selecting a second test vector as a vector having a lowest power-plane quiescent current value at a predetermined operating voltage from among a set of test vectors.

13. (Original) The computer program product of Claim 8, wherein said program instructions for evaluating comprise program instructions for:

determining whether or not a power-plane voltage corresponding to said change in linearity is above a

predetermined threshold; and

in response to determining that voltage is above said predetermined threshold, rejecting said integrated circuit as a failure.

14. (Original) The computer program product of Claim 8, wherein said program instructions further comprise program instructions for selecting said test vector as a vector having a highest power-plane quiescent current value at a predetermined operating voltage from among a set of test vectors.

15. (Currently Amended) A workstation comprising:

a memory for storing program instructions and data values for evaluating a shorting defect in an integrated circuit;

a processor for executing said program instructions, wherein said program instructions comprise program instructions for:

reading a plurality of quiescent power-plane current values at a plurality of corresponding power-plane voltages for a test vector for which said shorting defect is activated;

detecting a change in linearity of said plurality of power-plane current values with respect to said power-plane voltages;

determining a particular power-plane voltage above which said program instructions for detecting detect that said plurality of power-plane current values are linear with respect to said power-plane voltages; and

evaluating a level of severity of said shorting defect, wherein said level of severity is determined

in conformity with said particular power-plane voltage ~~a result of said detecting~~.

16. (Canceled).

17. (Currently Amended) The workstation of Claim 17 ~~16~~, wherein said program instructions further comprise program instructions for:

computing a first derivative of said quiescent power-plane current values at multiple ones of said power-plane voltages; and

detecting a peak value of said computed first derivative, and wherein said program instructions for determining determine ~~a lower bound of said range~~ said particular power-plane voltage as a voltage corresponding to said peak value.

18. (Original) The workstation of Claim 15, wherein said program instructions further comprise program instructions for:

second reading a second plurality of quiescent power-plane current values at said plurality of power-plane voltages for a second test vector for which said shorting defect is not activated; and

subtracting said second plurality of quiescent power-plane current values from said plurality of quiescent power-plane current values read by said reading, whereby said plurality of quiescent power-plane current values are normalized, and wherein said program instructions for detecting operate on said normalized quiescent power-plane current values.

19. (Original) The workstation of Claim 18, wherein said

program instructions further comprise program instructions for selecting a second test vector as a vector having a lowest power-plane quiescent current value at a predetermined operating voltage from among a set of test vectors.

20. (Original) The workstation of Claim 15, wherein said program instructions for evaluating comprise program instructions for:

determining whether or not a power-plane voltage corresponding to said change in linearity is above a predetermined threshold; and

in response to determining that voltage is above said predetermined threshold, rejecting said integrated circuit as a failure.

21. (Original) The workstation of Claim 15, wherein said program instructions further comprise program instructions for selecting said test vector as a vector having a highest power-plane quiescent current value at a predetermined operating voltage from among a set of test vectors.